Please amend the following:

IN THE SPECIFICATION:

At page 1, line 3, please delete the existing Title and replace with the following amended Title:

SEMICONDUCTOR STORAGE APPARATUS

At page 4, line 16, please replace JP-A-2002-156184 with the following:

JP-A-2003-257175

At page 4, beginning at line 18, please replace paragraph with the following amended paragraph:

Disclosure of Invention

The magnetization reversal time of a magnetic substance is as fast as one nanosecond or less. Therefore, it is one of merits of the MRAM that fast writing is possible in principle. Since the write current of the MRAM is required to be accurate as described in the description of the ~~conventional technology~~ background art above, however, it is necessary to use a constant current source as the write current source. In the conventional constant current write circuit described above, electric charges are stored on parasitic capacitors which are present on wire and in selectors immediately after the write current source is turned on. Therefore, a certain time is needed until a constant current actually flows in the position of the selected cell at the selected bit line BL 905 and the selected word line WL 906. This results in a problem that power consumption at the time of writing increases. This problem will now be described with reference to FIGS. 18 to 21. FIG. 18 shows a memory cell array (four by four cells are shown.). A

constant current source circuit is prepared on each of the X side and Y side. Ideally, as shown in FIG. 19A, constant currents ICX and ICY output from the constant current sources flow in the array without any change, as constant currents IAX and IAY. Therefore, it is anticipated that the write current rises in no time. However, parasitic capacitors CLX, CLY, CX1,..., CXm, CY1,..., CYm are present in the actual circuit (in the case of m-row m-column array) as shown in FIG. 18. Even if the constant current sources let the constant currents ICX and ICY flow outside the array, a current in the array is dissipated to charge the parasitic capacitors especially immediately after the current is flowed. As a result, the current waveform becomes dull as shown in FIG. 19B. Especially in the case of the MRAM, a current having a specific value or less does not have writing capability and consequently it is necessary to wait until the current value reaches a necessary value. Therefore, fast writing becomes difficult and a wasteful current is caused as represented by a shaded portion in FIG. 19B. Especially in the case of the MRAM, therefore, there is a drawback that the power consumption increases because the write current value is large (several mA).

At page 8, lines 15 – 20, please replace with the following amended paragraph:

In addition, in the boost circuit in the present semiconductor memory device, the boost capacitor is divided in order to form a geometric progression according to a selection pattern. Therefore, all boost capacitors are used at the time of maximum boost (writing to the remotest array, [[the]] with maximum current). As a result, waste does not occur in the area occupied by the boost capacitor and the area occupied by the array can be increased.

At page 9, lines 2 – 14, please replace with the following amended paragraphs:

In the semiconductor memory device, the storage element may be a tunnel magnetoresistance element, and the predetermined position may be a position, ~~where~~ a ~~magnetic~~

~~field by a~~ current at which generates a magnetic field [[is]] applied to the tunnel magnetoresistance element.

In the semiconductor memory device, the boost circuit may include a condenser for storing charge to charge the parasitic capacitors.

The semiconductor memory device may further include a circuit for setting a voltage between both electrodes of the condenser to a voltage greater than ~~or equal to~~ a power supply voltage.

In the semiconductor memory device, ~~a plurality of the condensers may be provide~~ the condenser may be increased to a plurality of condensers, and the boost circuit may include switching means for ~~switching a condenser~~ selecting one or more condensers to be used for charging, according to an amount of charge required to charge the parasitic capacitors.

At page 10, lines 5 – 10, please replace with the following amended paragraph:

The semiconductor memory device according to the present invention includes returning means for returning at least a part of charge on parasitic capacitors which are present on a current path of a current for writing information into the storage element, to a node where charge of the boost circuit is stored. Therefore, an MRAM having low current dissipation can be obtained.

At page 10, lines 16 – 21, please replace with the following amended paragraph:

The semiconductor memory device according to the present invention includes retention means for retaining a part of charge on parasitic capacitors which are present on a current path of a current for writing information into the storage element, in dependence on history of an operation mode, so as to suppress discharge of the boost circuit. Therefore, an MRAM having low current dissipation can be obtained.

At page 14, lines 26 – 27 and page 15, lines 1-14, please replace with the following amended paragraph:

If the constant current source circuit ~~enters~~ 103 the operation state and the signal WENX and the signal VBSTX are switched from the L level to the H level (Vdd), the PMOS transistor MBX turns off and the PMOS transistor MSX turns on. A potential at the node VBX is approximately equal to the power supply voltage Vdd. A potential on wire NLX is lower than ~~or equal~~ to the power supply voltage Vdd, and it is equal to, for example, GND. Therefore, charge stored on the boost capacitor CBX abruptly flows through the selected wire. This current is an instantaneous overshoot current reflecting the discharge phenomenon, and flows for several nanoseconds while charging the parasitic capacitors CLX, CX1,..., CXm. If the potential at the node VBX soon becomes equal to the wire potential NLX, the flow of the boost current ceases. This situation is indicated by a current waveform IBX shown in FIG. 3B. While the signal VBSTX is at the H level, a potential drop of ΔVBX occurs at the node VBX. On the contrary, the potential NLX on the selected wire rises from the GND potential to Vdd-ΔVBX.

At page 15, lines 15 – 26, please replace with the following amended paragraph:

If the boost circuit 101 were off, a current from the X side write constant current source circuit 103 would flow into the parasitic capacitor, and therefore, a rising edge of the current IAX at the wire terminus would become dull (see IAX shown in FIG. 3B). ~~However, in a case where~~ On the other hand, because the boost circuit 101 is on, the parasitic capacitor can be charged by the boost current IBX as described above and consequently the dullness in the current waveform decreases. If the capacitance of the boost capacitor CBX is adjusted to a proper value in the design, the current IAX = ICX + IBX that actually flows through the cell array can be made to rise in a short time (approximately 2 nanoseconds) as shown in ~~a signal in~~ the bottom row in FIG. 3B. Therefore, writing is completed in a short time, and the power consumption can be

prevented from being increased.

At page 18, lines 15 – 27, and page 19, lines 1-3, please replace with the following amended paragraph:

If the constant current source circuit 103 enters the operation state and a write start signal WENX and a boost start signal VBSTX are switched from the L level to the H level, the PMOS transistor MBX turns off and the PMOS transistor MSX turns on. A potential at the node VBX immediately before the switching is approximately equal to a boosted voltage VBT. A potential on wire NLX is lower than ~~or equal to~~ the VBT, and it is equal to, for example, the ground potential. The moment MSX turns on, therefore, charge stored in the boost capacitor CBX abruptly flows through the selected wire. This current is an instantaneous overshoot current and flows for several nanoseconds while charging parasitic capacitors CLX, CX1,..., CXm. If the potential at the node VBX soon becomes equal to the wire potential NLX, the flow of the boost current ceases. This situation is indicated by current waveforms shown in FIG. 6B. While the signal VBSTX is ~~ON~~ at the H level, a potential drop of ΔVBX occurs at the node VBX. On the contrary, the potential NLX on the selected wire rises from the GND potential to VBT-ΔVBX.

At page 18, lines 7 – 18, please replace with the following amended paragraph:

If the boost circuit 101B were off, a current from the X side write constant current source circuit 103 would flow into the parasitic capacitor, and therefore, a rising edge of the current IAX in the array would become dull (see FIG. 6B). ~~However, in a case where~~ On the other hand, because the boost circuit 101B is on, the parasitic capacitor can be charged by the boost current IBX as described above and consequently the dullness in the current waveform decreases. If the

capacitance of the boost capacitor CBX is adjusted to a proper value in the design, the current IAX = ICX + IBX that actually flows through the cell array can be made to rise in a short time (approximately 2 nanoseconds) as shown in the bottom row in FIG. 6B. Therefore, writing is completed in a short time, and the power consumption can be prevented from being increased.

At page 20, lines 6 – 25, please replace with the following amended paragraph:

It is supposed that an X side write constant current source 103 shown in FIG. 7 can output current values of n ways, i.e., IX1, IX2, ···, IXn. The reason is as follows. The magnetization reversal current of the MRAM varies according to the process condition or the like. Therefore, there is a possibility that the designed current value is not necessarily an optimum current value. Accordingly, it is necessary to adjust the current value at the time of manufacture and shipping. That is the reason. Since ~~the parasitic capacitor Qk~~ the amount Qk of charge stored in the parasitic capacitor changes according to the equation (1) depending upon the write current values of n ways, therefore, it is also necessary to prepare current boost capacitors of n ways. M small arrays XA1, ···, XAM are arranged in the X direction. In addition, the ~~the~~ amount Qk of chare stored in the parasitic capacitor ~~Qk~~ changes according to the equation (1) depending upon the X direction write array position k (k = 1, 2, ···, M) as well. Therefore, it is also necessary to prepare current boost capacitors of M ways. Further, since there is a possibility that the actual parasitic capacitor will differ from the design value, it is necessary to correct the current boost amount and to prepare boost capacitors of s ways for this purpose. If the X side capacitor array 111 in each row shown in FIG. 7 is formed of M × n × s capacitors to satisfy the needs heretofore described, there is a fear that the area occupied by the current boost capacitor will become enormous.

At page 20, lines 26 – 27, and page 21, lines1 - 11, please replace with the following amended paragraph:

However, if such a structure that the charge on all boost capacitors are used at the time of maximum boost (when the current is maximum, the remotest array is selected, and the correction boost amount is maximum) is adopted and capacitors are made to have relations represented by a geometric progression so as to be able to approximate the equation (1) of parasitic capacitors, then it is possible to decrease the number of boost capacitors, and hence the area occupied by the boost capacitor can be made small. For example, in the present embodiment, ~~shown in~~ FIG. 8 ~~are used as blocks of an~~ shows the X side capacitor array and blocks of the [[an]] X side capacitor selectors (As for the Y side as well, a similar configuration is possible). The block shown in FIG. 8 is prepared every row of the array. Here, the number of X direction write array positions = 4, the number of current values = 4, and the number of correction values s = 4.

At page 23, lines 2 – 27, and page 24, lines 1 - 22, please replace with the following amended paragraph:

"11" and "12" terminals in FIG. 9 respectively correspond to "11" and "12" terminals shown in FIG. 8, and they are used to adjust the boost amount according to the equation (1) depending upon the values of adjusted write constant currents. For example, when I1 = L and I2 = L, a boost capacitor (#1, #7, #13 or #19) connected to an output terminal C1 and a boost capacitor (#2, #8, #14 or #20) connected to an output terminal C2 in FIG. 9 become candidates for selection. When I1 = H and I2 = L, the boost capacitor (#1, #7, #13 or #19) connected to the output terminal C1, the boost capacitor (#2, #8, #14 or #20) connected to the output terminal C2, a boost capacitor (#3, #9, #15 or #21) connected to an output terminal C3, and a boost capacitor (#4, #10, #16 or #22) connected to an output terminal C4 in FIG. 9 become candidates for selection. When I1 = L and I2 = H, the boost capacitor (#1, #7, #13 or #19) connected to the output terminal C1, the boost capacitor (#2, #8, #14 or #20) connected to the output terminal C2, a boost capacitor (#5, #11, #17 or #23) connected to an output terminal C5 and a boost capacitor (#6, #12, #18 or #24) connected to an output terminal C4 in FIG. 9 become candidates for

selection. When I1 = H and I2 = H, the boost capacitor (#1, #7, #13 or #19) connected to the output terminal C1, the boost capacitor (#2, #8, #14 or #20) connected to the output terminal C2, the boost capacitor (#3, #9, #15 or #21) connected to the output terminal C3, the boost capacitor (#4, #10, #16 or #22) connected to the output terminal C4, the boost capacitor (#5, #11, #17 or #23) connected to the output terminal C5 and the boost capacitor (#6, #12, #18 or #24) connected to the output terminal ~~C4~~ C6 in FIG. 9 become candidates for selection.

"S1" and "S2" terminals in FIG. 9 correspond to the "S1" and "S2" terminals shown in FIG. 8 and are used to compensate the dependence of the charge Qk stored in the parasitic capacitor ~~Qk~~ upon the process condition. For example, when S1 = L and S2 = L, any boost capacitor is not selected. When S1 = H and S2 = L, the boost capacitor (#1, #7, #13 or #19) connected to the output terminal C1, the boost capacitor (#3, #9, #15 or #21) connected to the output terminal C3 and the boost capacitor (#5, #11, #17 or #23) connected to the output terminal C5 in FIG. 9 become candidates for selection. When S1 = L and S2 = H, the boost capacitor (#2, #8, #14 or #20) connected to the output terminal C2, the boost capacitor (#4, #10, #16 or #22) connected to the output terminal C4, and the boost capacitor (#6, #12 #18 or #24) connected to an output terminal C6 in FIG. 9 become candidates for selection. When S1 = H and S2 = H, the boost capacitor (#1, #7, #13 or #19) connected to the output terminal C1, the boost capacitor (#2, #8, #14 or #20) connected to the output terminal C2, the boost capacitor (#3, #9, #15 or #21) connected to the output terminal C3, the boost capacitor (#4, #10, #16 or #22) connected to the output terminal C4, the boost capacitor (#5, #11, #17 or #23) connected to the output terminal C5, and the boost capacitor (#6, #12, #18 or #24) connected to the output terminal C6 in FIG. 9 become candidates for selection.

IN THE ABSTRACT:

At page 32, please replace the existing paragraph with the following: